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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Alan R. Reinberg

Title: METHOD FOR REDUCING SINGLE BIT DATA LOSS IN A MEMORY CIRCUIT

Docket No.: 303.522US1
Filed: August 25, 1999
Examiner: Richard A. Booth

Serial No.: 09/382,442
Due Date: February 3, 2001(Saturday)
Group Art Unit: 2812

Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

X A return postcard.
X An Amendment and Response (4 Pages).

Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)

By: J. M. Kalis
Atty: Janal M. Kalis
Reg. No. 37,650

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 5th day of February, 2001.

JANAL M. KALIS
Name

J. M. Kalis
Signature

Customer Number 21186
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)
(GENERAL)

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PATENT

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AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

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Applicant has reviewed the Office Action mailed on November 3, 2000. Please amend the above-identified patent application as follows.

IN THE CLAIMS

Please amend the claims as follows:

A1

6. (Amended) The method of claim 1 and further comprising exposing the semiconductor layer, sequentially, to atmospheres comprising Hydrogen isotope and ammonia enriched in Hydrogen isotope at an elevated temperature.

Sub B4

26. (Amended) A method of forming a non-volatile electrically alterable semiconductor memory cell with reduced, random, single bit data loss in a memory circuit comprising:

providing a silicon substrate;

fabricating a field oxide region and a channel region over or within the silicon substrate;

growing an oxide over the channel region in an atmosphere

enriched in Hydrogen isotope;

fabricating at least one gate member; and

passivating the memory cell in an atmosphere that comprises Hydrogen

isotope.

Sub B5 A3

35. (Amended) A method for passivating a non-volatile, electrically alterable semiconductor memory cell, thereby reducing random, single bit data loss in a memory circuit, comprising:

providing a non-volatile, electrically alterable semiconductor memory cell;